Edited by Bill Travis

Data-acquisition system uses fault protection

Catherine Redmond, Analog Devices, Limerick, Ireland

SENSITIVE SYSTEMS, such as those in aircraft, must withstand fault conditions, thereby avoiding component and system damage, because a sensor failure could cause a catastrophic event to occur. A channel protector, comprising two n-channel MOSFETs connected in series with a p-channel MOSFET, can protect sensitive components from voltage transients in the signal path, whether or not the power supplies are present (**Figure 1**). The channel protector acts as series resistor during normal operation. If the input exceeds the power-supply voltages, one of the MOSFETs turns off, clamping the output within the supply rails, thus protecting the circuitry in the event of overvoltage or supply-loss conditions. Because channel protectors work regardless of the presence of the supplies, they are also ideal for applications in which correct power sequencing cannot be guaranteed and for hot-insertion rack systems. **Figure 2** shows an ADG465 channel protector with an input signal that exceeds the power-supply voltage. The protector clamps the output signal, protecting the sensitive components that follow the channel protector.

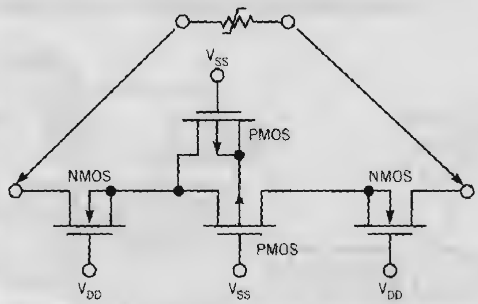
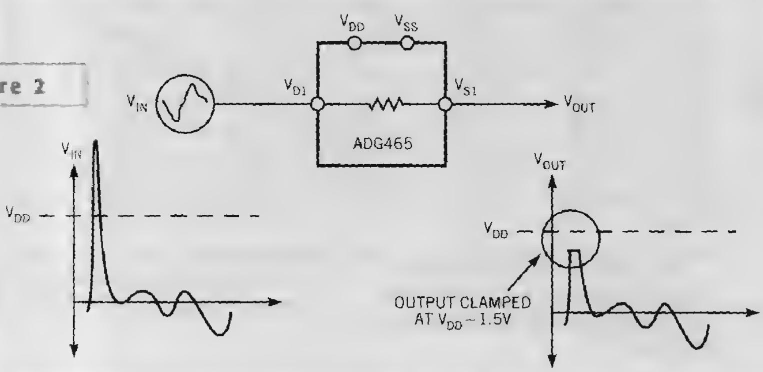


Figure 1 **A channel protector can protect sensitive circuitry from voltage transients.**

When a fault condition occurs, the voltage on the input of the channel protector exceeds a voltage set by the supply-rail voltage minus the MOSFET's threshold voltage. For a positive overvoltage, this voltage is $V_{DD}-V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistor (typically, 1.5V). In the case of a negative overvoltage, the voltage is $V_{SS}-V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (typically, −2V). When the input of the channel protector exceeds either of these voltages, the protector clamps the output within them. These devices offer bidirectional fault and overvoltage protection, so you can use the inputs or outputs interchangeably. **Figure 3** shows the voltages and MOSFET states for a positive-overvoltage event.

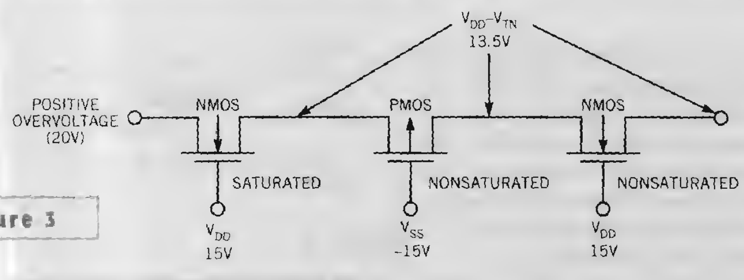
The output load limits the current during the fault condition to V_{CLAMP}/R_L (**Figure 4**). If the supplies are off, the protector limits the fault current to nanoamps. **Figure 5** shows how you can use the ADG466 channel protector to protect the sensitive inputs of an instrumentation amp from a sensor fault. In applications that require a multiplexer in

Figure 2



The channel protector clamps overvoltage transients to a safe level.

Figure 3



The voltages and MOSFET states appear like this during a positive-overvoltage event.

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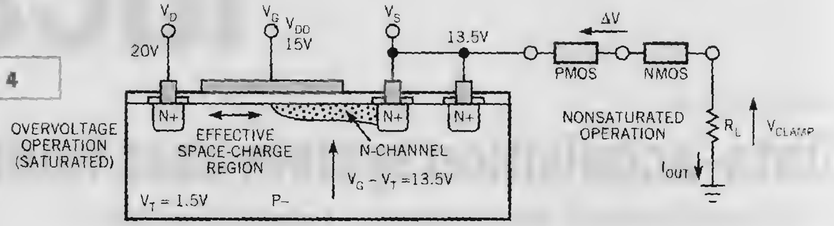
addition to channel protection, you can use the ADG439F fault-protected, four-channel analog multiplexer (**Figure 6**). These multiplexers use a series n-channel, p-channel, n-channel MOSFET connection. During fault conditions, the inputs or outputs appear as open circuits, protecting the sensor or signal source as well as the output circuitry.□

Figure 4



The output load limits the current to V_{CLAMP}/R_L during a fault condition.

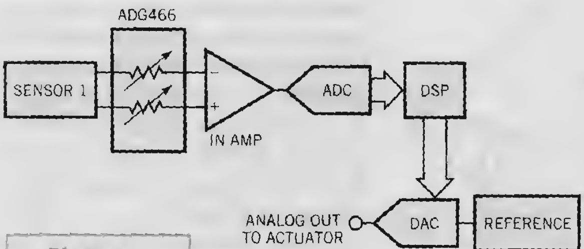


Figure 5

In this circuit, the ADG466 channel protector guards the sensitive inputs of an instrumentation amplifier from a sensor fault.

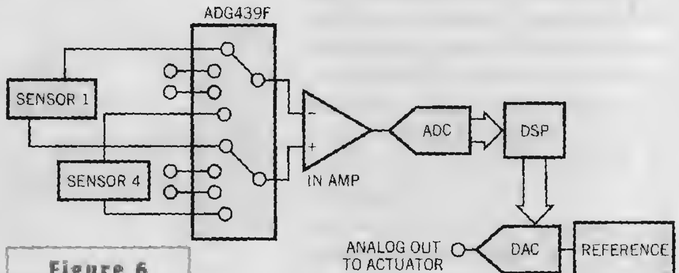


Figure 6

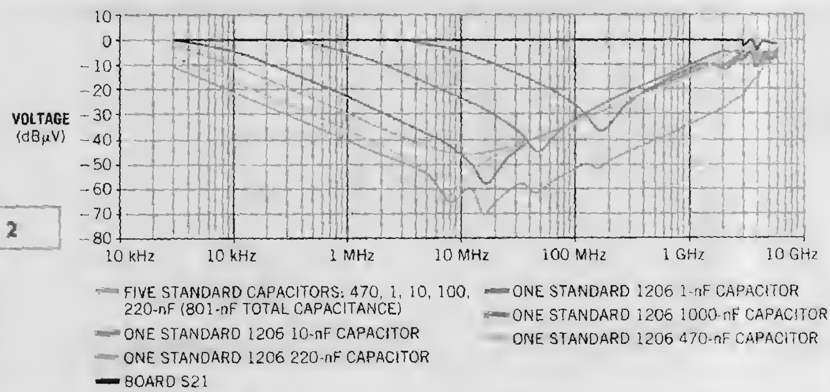
A multiplexer in a data-acquisition system protects the signal source as well as the output circuitry.

Take steps to reduce antiresonance in decoupling

Dale Sanders, X2Y Attenuators, LLC, Farmington Hills, MI

To maintain power integrity on pc boards, you need multiple capacitors to decouple the power-distribution system. A typical configuration might comprise five capacitors connected in parallel between the power and the ground traces or planes. To provide broadband decoupling performance, assume the individual values of the capacitors are 470, 1, 10, 100, and 220 nF (**Figure 1**). This parallel network provides 801-nF total capacitance to the power-distribution system. If you measure each capacitor with a vector-network analyzer, you can identify each capacitor's SRF (self-resonant frequency). **Figure 2** is a plot of each capacitor's SRF, as well as the SRF of the overall parallel connection. Each SRF can cause antiresonance in the parallel decoupling configuration. The antiresonance occurs when one capacitor is still capacitive, while another has become inductive.

Figure 2



Measurements with a vector-network analyzer reveal undesirable antiresonance effects.

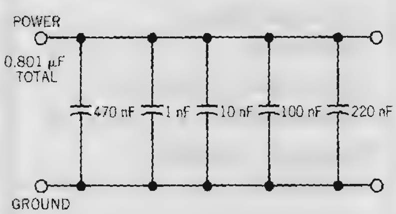


Figure 1

A typical decoupling configuration uses several multilayer-ceramic capacitors connected in parallel.

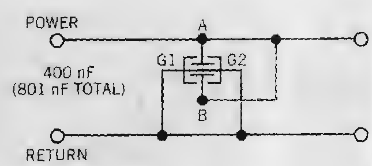
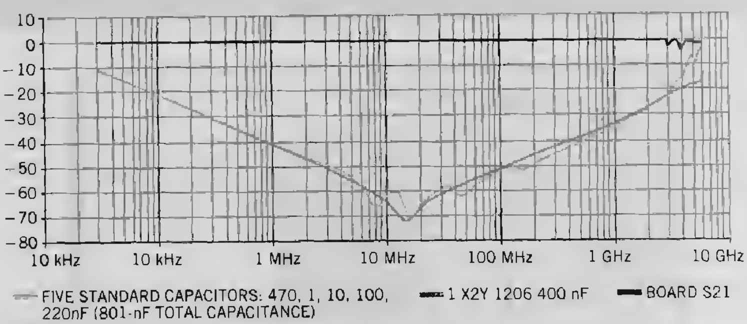


Figure 3

A 400-nF X2Y capacitor yields a total decoupling capacitance of 800 nF.

A way to considerably reduce the antiresonance effects is to use a single 400-nF X2Y capacitor for decoupling. (Capacitors using X2Y technology are available, for example, from Johanson Dielectrics (www.johansondielectrics.com). You measure the capacitance rating for an X2Y component from line to ground; in other words, from an A or a B terminal to either of the G1 or G2 terminals in **Figure 3**. So, the total capacitance a 400-nF X2Y component supplies, connected as in **Figure 3** would be double the capacitance rating, or 800 nF. **Figure 4** shows that a single X2Y capacitor with the same total capacitance as in **Figure 1** provides the same broadband decoupling as the standard decoupling configuration but without the antiresonance effects. In addition, because X2Y components come in the same package sizes as standard capacitors (1812, 1210, 1206, 0805, and 0603), the use of X2Y components saves pc-board space and reduces layout complexity.□

Figure 4



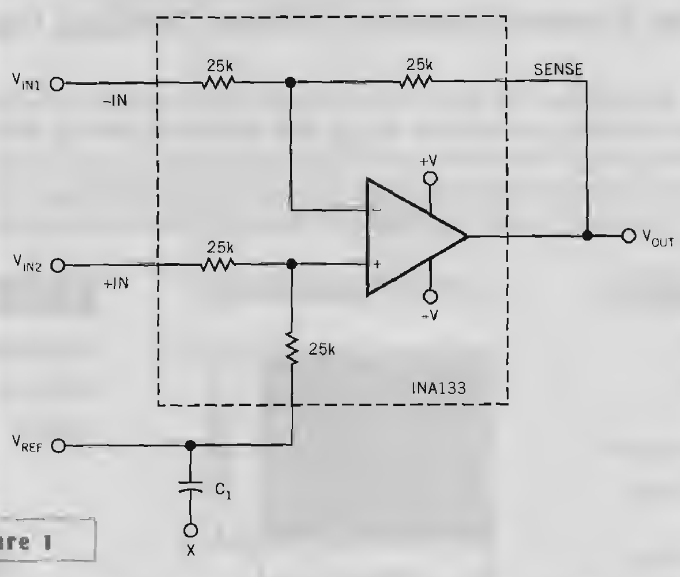
The single X2Y decoupling capacitor displays no antiresonance effects.

Precision level shifter has excellent CMRR

Ronald Mancini, Texas Instruments, Bushnell, FL

Most designers make level shifters with op amps and 1%-tolerance discrete resistors. Discrete-resistor mismatching limits the op amp's CMMR (common-mode rejection ratio) to 40 dB, so you cannot use op amps in circuits that require high CMRR. Differential amplifiers contain precision matched internal resistors, so ICs such as the INA133 can readily achieve CMRRs of approximately 90 dB. They can offer such high CMRR by trimming internal matched resistors. Assume that each input in the circuit of **Figure 1** has an associated noise voltage (V_{N1}, V_{N2}, and V_{NREF}). The transfer function of the amplifier circuit is $V_{OUT}=(V_{REF}+V_{NREF})+(V_{IN2}+V_{N2})-(V_{IN1}+V_{N1})$. Note that the reference voltage shifts the output signal, either single or differential. Once this level shifting occurs, you can turn your attention to the noise cancellation. Careful cabling and differentially coupling the signal into the differential amplifier's inputs force the noise on the signal inputs to be equal ($V_{N1}=V_{N2}$). The input noise is a common-mode signal, so the differential amplifier rejects it to the best of its ability (nominally, 90 dB). Now, $V_{OUT}=V_{IN2}-V_{IN1}+V_{REF}+V_{NREF}$.

Figure 1



C_1 allows the level shifter to act as a lowpass filter that rejects the reference noise.

Now, you need to eliminate the reference noise to obtain a clean level-shifted signal. You could connect the X end of C_1 to ground to shunt the reference noise to ground, but this solution may be ineffective because the source impedance of the reference is low. When, however, you connect the X end of C_1 to the V_{IN1} signal source, the differential amplifier acts as a lowpass filter and rejects the reference noise. This circuit keeps the input impedance of the differential amplifier low (approximately 25 kΩ for the INA133) to facilitate matching. Thus, you must keep the signal source impedance low to prevent gain errors. The source impedance should be less than 1/1000 the input impedance to minimize gain error. If this situation doesn't occur naturally, then it is best to buffer the inputs.□